R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for amended claims 1, 11 and 25 can be found in the drawings as originally filed (for example, in FIG. 3), and on page 11, lines 3-6 of the specification as originally filed.

CLAIM OBJECTIONS

The objection to claims 13 and 21 have been obviated by appropriate amendment and should be withdrawn.

Claims 13 and 21 have been modified for clarification purposes. Support for claim 13 can be found on page 26, lines 3-6 of the specification as originally filed. Support for claim 21 can be found on page 20, lines 15-18 of the specification as originally filed. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-25 under 35 U.S.C. §103 as being unpatentable over Levine et al. 5,970,439 (hereinafter Levine) is respectfully traversed and should be withdrawn.

Levine teaches performance monitoring in a data processing system (Title).

In contrast, claim 1 of the present invention provides an apparatus comprising a full system monitor. The monitor may be configured to monitor in real-time (i) one or more software variables down to change rates, (ii) one or more hardware registers down to cycle rates, and (iii) one or more firmware registers down to microcode fetch rates in response to one or more trigger signals. The one or more trigger signals may be generated by a first comparator circuit. Claim 24 provides similar limitations. Levine does not teach or suggest such a method or apparatus.

In particular, Levine does not teach a full system monitor configured to monitor in real-time (i) one or more software variables down to change rates, (ii) one or more hardware registers down to cycle rates, and (iii) one or more firmware registers down to microcode fetch rates. As noted by the Examiner, "Levine did not explicitly disclose software variable down to change rates, hardware registers down to cycle rates, and firmware registers down to microcode word fetch rates" (see page 4, lines 1-3 of the Office Action). The Office Action asserts that "Levine mentions fetching instructions as an item of interest" (see page 4, line 6). However, Levine is silent on monitoring fetch rates with a full system monitor. At best, Levine teaches a "fetch unit" or "fetch stage" with no reference made to monitoring fetch rates. The Office Action also asserts that "Levine discloses cycle and change rates" (see Office Action, page 4, line 7). However, Levine is

silent regarding monitoring change registers down to change rates and cycle rates. No such reference to change rates or cycle rates were found in Levine. Further, Levine fails to teach monitoring firmware registers down to microcode word fetch rates. The assertion in the Office Acton that "Levine intended for the entire data processing system to be monitored" is overly broad and conclusory at best. If Levine had intended for the entire data processing system to be monitored, one skilled in the art would expect to see at least some reference to monitoring change rates, cycle rates and microcode word fetch rates. No mention of such rates is found in Levine.

Finally, Levine fails to teach the presently claimed full system monitor configured to monitor in real time in response to a one or more trigger signals generated by a first comparator circuit. Levine is silent on a first comparator circuit configured to generate one or more trigger signals. Instead, Levine teaches a notification signal that is sent to the PM (Performance Monitor) from a time base facility (see Levine, page 9, lines 48-49). The Office Action asserts that "a negative counter . . . condition" (see Office Action page 8, line 7) is as a comparator. However, no such inference can be made by one skilled in the art. At best, the negative counter is part of the "time base facility 50 which includes a counter that designates a precise point in time for saving the machine state" (see Levine, column 9, lines 16-19).

Clearly, the counter of the time base facility is not the presently claimed first circuit comparator circuit. Therefore, the presently claimed invention is fully patentable over Levine and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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